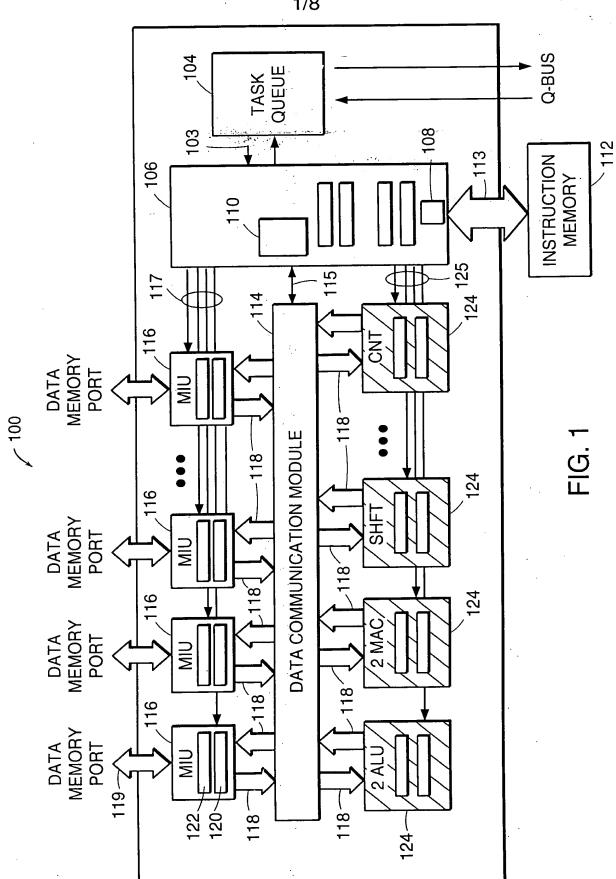
Designer Configurable Multi-Processor System by
Ussery et al.
Serial No.: 09/757,373
Atty Docket No.: IMP-002 (8326/5)
Atty/Agent: JVBianco (617) 248-7870
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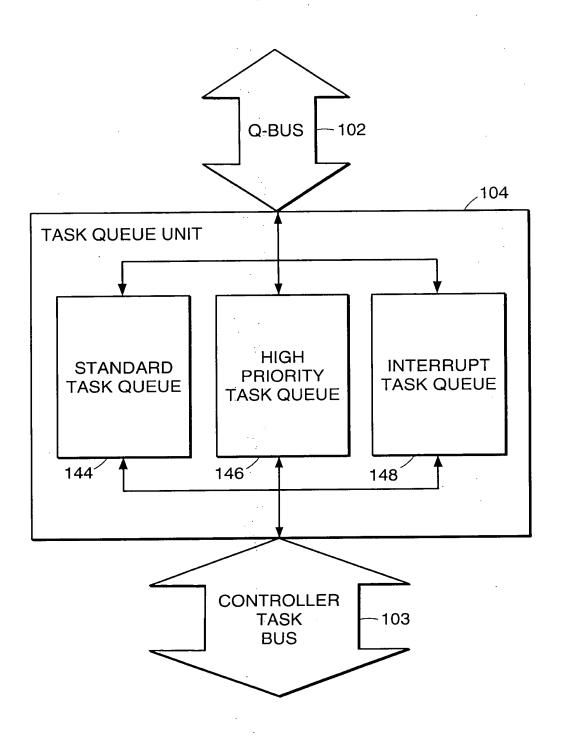


FIG. 2

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Serial No.: 09/757,373
Atty Docket No.: IMP-002 (8326/5)
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Sheet 3 of 8 3/8 INSTRUCTION MEMORY BUS 110 154 152 106 156 DECOMPRESSION INSTRUCTION INSTRUCTION REGISTERS CONSTANT CONTROL DECODE **BRANCH** CONTROLLER TASK BUS DATACOM CONTROL TASK CONTROLLER UNIT TASK MIU CONTROL CONTROL S162 — 166 160 168 DATACOM CONTROL BUS CU CONTROL BUS MIU CONTROL BUS 115 125

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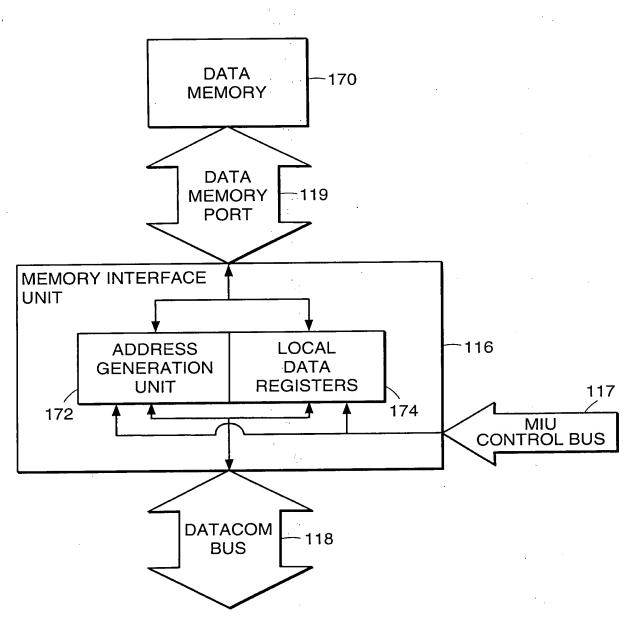


FIG. 4

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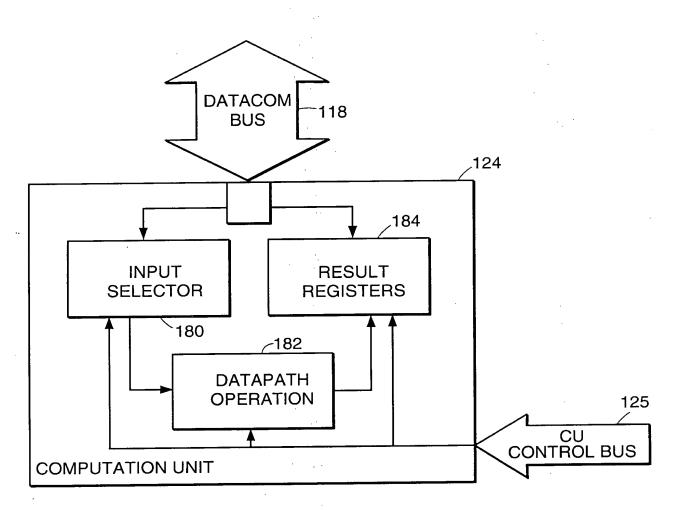


FIG. 5

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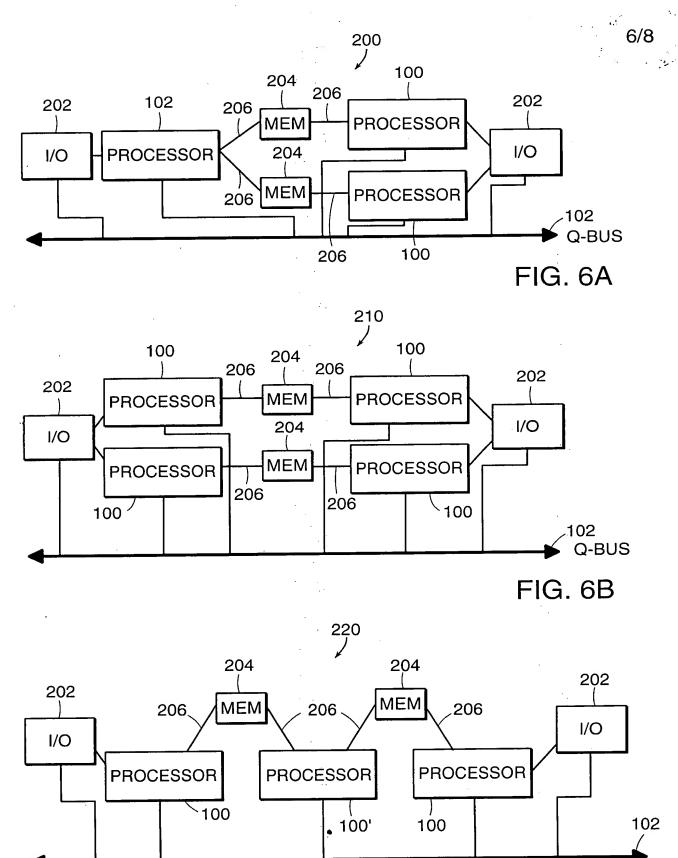


FIG. 6C

Q-BUS

Ussery et al.
Serial No.: 09/757,373
Atty Docket No.: IMP-002 (8326/5)
Atty/Agent: JVBianco (617) 248-7870
Sheet 7 of 8 7/8 (GENERAL OR VENDOR-SPECIFIC) 256 IMPLEMENTATION KIT 258 STANDARD ASIC/ IC DESIGN FLOW CONFIGURATION PLATFORM AND 252 **PROCESSOR** DEFINITION PLATFORM 250 SYSTEM INTEGRATION 268 270 PLATFORM MAPPING) 264 DEVELOPMENT ENVIRONMENT ENVIRONMENT (APPLICATION COMPILATION PROGRAM NOTATION BINARY IMAGE 262 254 **DEVELOPMENT BOARD APPLICATION** LIBRARY SET SIMULATOR (FPGA AND PSA) INSTRUCTION REHERSAL 266 < (ISS)

272

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Designer Configurable Multi-Processor System by Ussery et al.
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